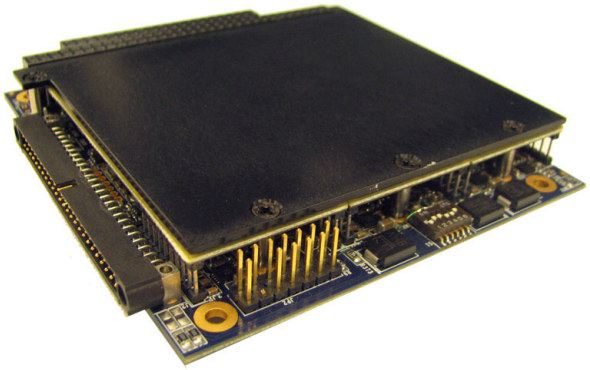
PC/104 THREE CHANNEL DIGITAL to SYNCHRO/RESOLVER CONVERTER

1.2 VA, 16 BIT RESOLUTION; 0.0167° ACCURACY; Built-In SELF TEST
With OPTIONAL ON-BOARD REFERENCE SUPPLY and PROGRAMMABLE DIGITAL I/O

FEATURES

- Three D/S(R) Channels
- 1 arc-minute accuracy
- 16 bit resolution
- 1.2 VA (maximum) drive capability per channel.
- Automatic background BIT testing continually checks and reports the health of each channel.
- Wrap-around S/D for reading actual commanded output angle.
- No adjustments or trimming required.
- Wide Operating Temperature Range.
- Software Support Kit and Drivers are available.



Typical Configuration Photo

DESCRIPTION

This PC-104 compliant stack through module incorporates (up to) three isolated Digital-to-Synchro/Resolver converters with 1.2 VA drive capability, continuous background BIT testing, reference and Signal loss detection and an optional reference supply. Each channel is independent, isolated and enables the user to ground one of the outputs without affecting performance. This model drives passive loads. In addition, the card provides programmable digital I/O capabilities and an optional on-board reference supply.

Major diagnostic capabilities offer substantial improvements to system reliability because user is immediately alerted to malfunctions. Two different tests (one on-line and one off-line) can be selected:

The (D2) test initiates automatic background bit testing (on-line) that compares the output of each channel against the commanded input to a test accuracy of 0.2° and monitors each Output and Reference with the results available from registers. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of this card and status reporting can be enabled or disabled.

The (D3) when enabled starts an initiated bit test that generates and tests 24 different angles (off-line) to a testing accuracy of 0.2°. External reference is required. Testing requires no external programming, and can be enabled or disabled via the bus.

CAUTION: Outputs are active during this (D3) test. Check connected loads for possible interference.

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SPECIFICATIONS

D/S(R) Channels

(for each channel unless otherwise specified)

Resolution:	16 bits (.0055°)
Accuracy:	±1 arc minutes (.0167°) at 1.2 VA. (No load to full load)
Output format:	Synchro or Resolver, Isolated
Output voltage:	2.0 - 11.8 Vrms, 2.0 – 28.0 Vrms 28.0 – 90.0 Vrms (programmable)
Output load:	1.2 VA maximum @ 11.8, 26 or 90 Vrms (power de-rates linearly with voltage) Short circuit protected
Regulation:	10% max. No load to Full load
Reference voltage:	2.0 – 115.0 Vrms (An optional on-board reference may be specified)
Reference frequency:	47 Hz to 10 KHz
Phase shift:	0.5° max. between output and reference (phase shift is programmable)
Rotation:	Programmable Start and Stop angles. 0 rps to 13.5 rps with a resolution of 0.15°/sec. Stepping rate is 16 bits to 3.4 rps, then is reduced to 14 bits up to 13.5 rps
Settling time:	Less than 100 µs
Power:	+5V @ 250 mA (quiescent, no-load) ± 12V @ 100 mA (quiescent, no-load) (per channel) 1.2 VA Full Load (adds ± 12V @ 220 mA average / ± 12V @ 310 mA peak per channel) Note: External +/- 12 VDC power may be configured/utilized (see part number)
Wrap around and Self Test:	Two different powerful test methods are detailed in the programming section.
Temperature:	Operating: -40°C to +85°C; Storage: -55°C to +105°C.
Size:	3.6 x 3.8 x 0.6
Weight:	12 oz.

Reference Supply

Optional. (May be specified in Slot 3 only - See part number configurator).

Voltage:	2.0 - 28 Vrms or 28 - 115 Vrms (programmable). Accuracy ±2%; (see part number). This factory set option is made available to maximize the available output power at lower output voltages. With a 26 Vrms or 115 Vrms output voltage, the maximum available output power is 3 VA that reduces linearly with reduced output voltage.
Frequency:	47 Hz to 10 Khz ±1% with 1 Hz resolution.
Regulation:	10% max. (No load to full load)
Output power:	3.0 VA max. (26 Vrms or 115 Vrms) (Reduces linearly with reduced output voltage).
Power:	+5V @ 300 mA (quiescent, no-load) ± 12V @ 150 mA (quiescent, no-load) 3.0 VA (max) Full Load (adds ± 12V @ 350 mA average / ± 12V @ 495 mA peak) Note: Reference supply module option may only be specified in Slot 3 (see part number configurator).
Ground:	Isolated from system ground

Digital I/O

8 Channel, Programmable as input or output. TTL and CMOS compatible. Includes bus hold. Therefore, when used as inputs, no external pull-up or pull-down resistors are required.

Vout L:	0.55 V max. at IOL of 64 mA max.
Vout H:	2.0 V min. at IOH of 32 mA max.
Vout H:	3.0 V min. at IOH of 3 mA
Vin L:	0.8 V
Vin H:	2.0 V
Vin max.:	5.0 V

PROGRAMMING INSTRUCTIONS

This card offers many options. Any option that is not required may be ignored. For ease of usage, all channels are referred to from 1 to 3. For two-speed applications we generally refer to Coarse and Fine inputs. Therefore, channel 1 is Coarse and channel 2 is Fine (channel 3 is configured individually as a single channel – ratio 1).

I/O Configuration

The card is addressed and accessed via 16-bit ISA/PC104 address/data format.
This card requires 32 consecutive addresses in the I/O address space on a 32 byte boundary. The base address is switch settable (utilizing S1 Dip Switch) in the 000-3E0 hex (0 to 992) address range (note mechanical layout).

ADDRESS= BASE + OFFSET

NOTE: Base addresses to avoid:

378-37F	Parallel Printer Port	3B0-3BF	Monochrome Display	3F8-3FF	Asynch Comm I/O	3F0-3F7	Floppy Disk

Register Bit Map

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Data (°) Hi	180	90	45	22.5	11.25	5.625	2.813	1.406	.703	.352	.176	.088	.044	.022	.011	.0055
Data (°) Lo	.00274	.00137	.00068	.00034	.00017	.00008	.00004	.00002	X	X	X	X	X	X	X	X
Active channels	X	X	X	X	X	X	X	X	X	X	X	X	X	Ch.3	Ch.2	Ch.1
Test Enable	X	X	X	X	X	X	X	X	X	X	X	X	D3	D2	X	X
Status, Reference	X	X	X	X	X	X	X	X	X	X	X	X	X	Ch.3	Ch.2	Ch.1
Status, Signal	X	X	X	X	X	X	X	X	X	X	X	X	X	Ch.3	Ch.2	Ch.1
Status, Test	X	X	X	X	X	X	X	X	X	X	X	X	X	Ch.3	Ch.2	Ch.1

Page-Specific Register Map

Page 1 (1E = 0)

00	Ch.1 Wrap Data Lo	R	08	Ch.3 Wrap Data L	R	10	-N/A-		18	-N/A-	
02	Ch.1 Wrap Data Hi	R	0A	Ch.3 Wrap Data Hi	R	12	-N/A-		1A	-N/A-	
04	Ch.2 Wrap Data Lo	R	0C	-N/A-		14	-N/A-		1C	-N/A-	
06	Ch.2 Wrap Data Hi	R	0E	-N/A-		16	-N/A-		1E	Page Register = 0	W/R

Page 2 (1E = 1)

00	Ch.1 D/S Angle Lo	W/R	08	Ch.3 D/S Angle Lo	W/R	10	Ch.3 D/S Filter	W/R	18	Ch.2 D/S Phase	W/R
02	Ch.1 D/S Angle Hi	W/R	0A	Ch.3 D/S Angle Hi	W/R	12	Ch.2/1 Ratio	W/R	1A	Ch.3 D/S Phase	W/R
04	Ch.2 D/S Angle Lo	W/R	0C	Ch.1 D/S Filter	W/R	14	-N/A-		1C	-N/A-	
06	Ch.2 D/S Angle Hi	W/R	0E	Ch.2 D/S Filter	W/R	16	Ch.1 D/S Phase	W/R	1E	Page Register = 1	W/R

Page 3 (1E = 2)

00	Ch.1 Stop Angle	W/R	08	Ch.1 Rot Rate Hi	W/R	10	Ch.3 Rot Rate Hi	W/R	18	-N/A-
02	Ch.2 Stop Angle	W/R	0A	Ch.2 Rot Rate Lo	W/R	12	D/S Rotation Mode	W/R	1A	-N/A-
04	Ch.3 Stop Angle	W/R	0C	Ch.2 Rot Rate Hi	W/R	14	D/S Start Rotation	W/R	1E	-N/A-
06	Ch.1 Rot Rate Lo	W/R	0E	Ch.3 Rot Rate Lo	W/R	16	D/S Stop Rotation	W/R	1E	Page Register = 2 W/R

Page 4 (1E = 3)

00	Ch.1 Ref Volt Lo	W/R	08	Ch.3 Ref Volt Lo	W/R	10	Ch.2 Sig Volt Lo	W/R	18	D/S Output Mode	W/R
02	Ch.1 Ref Volt Hi	W/R	0A	Ch.3 Ref Volt Hi	W/R	12	Ch.2 Sig Volt Hi	W/R	1A	-N/A-	
04	Ch.2 Ref Volt Lo	W/R	0C	Ch.1 Sig Volt Lo	W/R	14	Ch.3 Sig Volt Lo	W/R	1C	-N/A-	
06	Ch.2 Ref Volt Hi	W/R	0E	Ch.1 Sig Volt Hi	W/R	16	Ch.3 Sig Volt Hi	W/R	1E	Page Register = 3	W/R

Page 5 (1E = 4)

00	Ch.1 Trig Source	W/R	08	-N/A-		10	-N/A-		18	-N/A-	
02	Ch.2 Trig Source	W/R	0A	-N/A-		12	-N/A-		1A	-N/A-	
04	Ch.3 Trig Source	W/R	0C	-N/A-		14	-N/A-		1C	-N/A-	
06	Trigger Slope	W/R	0E	-N/A-		16	-N/A-		1E	Page Register = 4	W/R

Page 6 (1E = 5)

00	Ch.1 VLL Thresh	W/R	08	Ch.2 VREF Thresh	W/R	10	-N/A-		18	-N/A-	
02	Ch.2 VLL Thresh	W/R	0A	Ch.3 VREF Thresh	W/R	12	-N/A-		1A	-N/A-	
04	Ch.3 VLL Thresh	W/R	0C	-N/A-		14	-N/A-		1C	-N/A-	
06	Ch.1 VREF Thresh	W/R	0E	-N/A-		16	-N/A-		1E	Page Register = 5	W/R

Page 7 (1E = 6)

00	Active Chan Select	W/R	08	Status, Test BIT Fail	R	10	Ch.3 VLL (Read)	R	18	Ch.1 RefFREQ (Read)	R
02	Status, Reference Loss	R	0A	Status, Signal Loss	R	12	Ch.1 VRef (Read)	R	1A	Ch.2 RefFREQ (Read)	R
04	Status, Phase Lock Loss	R	0C	Ch.1 VLL (Read)	R	14	Ch.2 VRef (Read)	R	1C	Ch.3 RefFREQ (Read)	R
06	Status, Rotation	R	0E	Ch.2 VLL (Read)	R	16	Ch.3 VRef (Read)	R	1E	Page Register = 6	W/R

Page 8 (1E = 7)

00	OSC Volt	W/R	08	DIO 0-7 I/O Select	W/R	10	-N/A-		18	-N/A-	
02	OSC Freq Lo	W/R	0A	DIO Output	W/R	12	-N/A-		1A	-N/A-	
04	OSC Freq Hi	W/R	0C	DIO Input	W/R	14	-N/A-		1C	-N/A-	
06	-N/A-		0E	-N/A-		16	-N/A-		1E	Page Register = 7	W/R

Page 9 (1E = 8)

00	Version, Mod Design	R	08	ID, Mod (Part Number)	R	10	Watchdog Timer	R	18	Power Enable	W/R
02	Revision, Mod Design	R	0A	Serial Number	R	12	Soft Reset	R	1A	-N/A-	
04	Revision, DSP	R	0C	Date Code	R	14	Board Ready	R	1C	Test Enable	R
06	Revision, FPGA	R	0E	-N/A-		16	Test (D2) Verify	W/R	1E	Page Register = 8	W/R

Page(s) 10 - 15 (1E = 9 -E) PENDING (RESERVED)

WRAP (S/D) SPECIFIC REGISTERS

Wrap S/D Angle (Read)

Read individual channels 1, 2 or 3.

Register Bit Map

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Data (°) Hi[1]	180	90	45	22.5	11.25	5.625	2.813	1.406	.703	.352	.176	.088	.044	.022	.011	.0055
Data (°) Lo[1]	.00274	.00137	.00068	.00034	.00017	.00008	.00004	.00002	X	X	X	X	X	X	X	X

D/S Channel V_{L-L}

Each individual channel output signal voltage "V_{L-L}" is measured and the value reported to a corresponding read register. The input voltage is reported to a resolution of 10 mv rms. The output is in integer decimal format. For example, if channel 1 input signal voltage is 11.8 Vrms, the output measurement word from the corresponding register would be 1180 (0x49C).

D/S Channel VREF

Each individual channel input signal voltage "VREF" is measured and the value reported to a corresponding read register. The input voltage is reported to a resolution of 10 mv rms. The output is in integer decimal format. For example, if channel 1 input signal voltage is 26.0 Vrms, the output measurement word from the corresponding register would be 2600 (0xA28).

D/S Channel REFFREQ

Each individual channel input Reference Frequency "REFFREQ" is measured and the value reported to a corresponding register. The output reference frequency is programmed to a resolution of 1 Hz. The commanded output word is in integer decimal format. For example, if the reference frequency is 400 Hz, the output measurement word from the corresponding register would be 400 (0x190).

STIMULUS D/S SPECIFIC REGISTERS

D/S Write Angle – Single Speed:

For single-speed applications (Ratio=1), write a 16-bit integer (or 16-bit 2's compliment integer) to the corresponding channel *D/S Data Register.* (ex. 330° = EAABh).

WORD = (Angle ÷ (360/2^{16})).

Note: Writing to an Input Angle Register will stop any rotation initiated on that channel

D/S Write Angle – Two Speed

The dual channel module can automatically simulate two-speed applications (applies only to dual channel modules). Write an "up to" 24-bit integer (24-bit 2's compliment integer) to the corresponding channel *D/S Write Angle Register* to the coarse (channel 1) channel. By entering a ratio in the *D/S Ratio 1/2 register*, the fine (channel 2) channel will automatically output a signal proportional to the programmed coarse channel times the ratio programmed.

D/S Response / Filter Time

The D/S Response/Filter Time register controls the "soft start" or "ramp" to change the output signal from one angle to another. "0" is default and sets this filter time to "off". "1" is the slowest time where "FFFF" would be the quickest time.

D/S Ratio

Enter the desired ratio, as an integer number in the *D/S Ratio Register* corresponding to the pair of channels to be used as a two-speed channel (only applies for channels 1, 2). Example: Single speed = 1; 36:1 = integer 36. (Ratio range from 1 to 255).

D/S Phase

The phase of each individual channel may be offset from Reference. The phase may be adjusted at a resolution of 0.1 deg / bit. Program the desired lead or lag in integer as a 2's complement word format. For example, if channel 1 output signal is to lead the reference signal by 1.6 degrees, program the corresponding channel phase register to 16 (10h). If channel 1 output signal is to lag the reference signal by 1.6 degrees, program the corresponding channel phase register to -16 (FFF0h). Phase shift range is -90 <= x <= 90.

D/S Stop Angle

Stop Angles: Write the desired stop angle to appropriate channel Stop Angle Register. After a channel reaches the stop angle, it will stop rotating and remain at that angle until a new input angle is set. If rotation is initiated again, the angle will start rotating from the present angle.

Rotation Rate

Write to the corresponding Rotation Rate Register a 2's compliment number representing the desired rotation rate, LSB = 0.15°/sec.

Ex: 12 RPS =. (12 x 360°/0.15° = 28800 = 7080h), -12 rps = (-12 x 360°/0.15° = -28800 = 8F80h)

Step size is 16 bits (0.0055°) for up to 1.5 rps, then linearly increases to 12 bits (0.088°) at 13.6 rps.

Start Rotation

First set the *Rotation Rate* and *Rotation Mode* Registers for each channel that is to rotate. Then, to start rotation for the corresponding channel, write a "1" to the corresponding channel *D/S Start Rotation* register.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Start Rotation	X	X	X	X	X	X	X	X	X	X	X	X	X	CH3	CH2	CH1

Stop Rotation

To stop rotation for the corresponding channel, write a "1" to the corresponding channel *D/S Stop Rotation* register. Channel will remain at the stopped angle until new input angles are set, or rotation is again initiated. Note: An in-process rotation can also be stopped by commanding a new angle (*D/S Write Angle*).

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Stop Rotation	X	X	X	X	X	X	X	X	X	X	X	X	X	CH3	CH2	CH1

D/S Rotation Mode, Continuous or Start/Stop

For continuous rotation, set the corresponding channel bit to "0" (default) in the *Rotation Mode Register*. For rotation to cease at a designated stop angle, set the bit to "1". For 2-speed applications, only the odd or coarse channel needs to be programmed (CH1) (2-speed does not apply for CH3). Note corresponding trigger command registers for rotation start options.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Rotation Mode	X	X	X	X	X	X	X	X	X	X	X	X	X	CH3	CH2	CH1

D/S Channel Reference Voltage

Each individual channel input Reference voltage "VREF" must be programmed with the expected input Reference voltage supplied. The input REF voltage is programmed to a resolution of 10 mv rms. The command is in integer decimal format. For example, if channel 1 input REF voltage is 11.8 Vrms, the Reference input voltage would be programmed to the corresponding register with 1180.

D/S Channel Signal Voltage

Each individual channel output signal voltage "V_{L-L}" is programmed in a corresponding register. The signal output voltage is programmed to a resolution of 10 mv rms. The command is in integer decimal format. For example, if channel 1 input signal voltage is to be set for 11.8 Vrms, the command word to the corresponding register would be 1180.

D/S Output Mode

The D/S Output Mode register is utilized for selecting either ratio-metric or fixed mode voltages. Ratio-metric Mode, when selected, will cause the output signal voltage of the channel to vary with the input Reference Voltage applied. Fixed Mode, when selected, will set the channel voltage at a particular voltage chosen and set in the D/S Signal Voltage register regardless of the actual input reference voltage applied. Set register to "0" for Ratio-metric Mode. Set register to "1" for Fixed Mode.

D/S Trigger Source Select

(Internal = "29(h)"; External = "28(h)")
Enter Trigger Source for each channel in respective register. Trigger commands apply to rotation start.

D/S Trigger Slope Select

(Positive = "0"; Negative = "1") When trigger source is set to "external", trigger will initiate upon slope selected. Trigger commands apply to rotation start.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Trigger Slope Select	X	X	X	X	X	X	X	X	X	X	X	X	X	CH3	CH2	CH1

D/S Power Enable

The D/S Power Enable controls the application of power to the output amp stage, in effect, enabling or disabling the output signal. Set the corresponding bit per channel to "1" to enable power; set to "0" to disable power.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D/S Power Enable	X	X	X	X	X	X	X	X	X	X	X	X	X	**CH3**	**CH2**	**CH1**

D/S V_{L-L} Threshold

Each individual channel V_{L-L} output is measured and compared with the value programmed to the *D/S V_{L-L} Threshold* register. If the V_{L-L} delivered is less than he value set in the *V_{L-L} Threshold* register, the corresponding bit in the V_{L-L} Signal Status register for the particular channel will be set. The D/S V_{L-L} threshold voltage is programmed to a resolution of 10 mv rms. The command is in integer decimal format. For example, if channel 1 input V_{L-L} Threshold is to be set for 6.0 Vrms, the command word to the corresponding register would be 600.

D/S VREF Threshold

Each individual channel VREF input is measured and compared with the value programmed to the *D/S VREF Threshold* register. If the VREF input measurement is less than he value set in the *VREF Threshold* register, the corresponding bit in the *Reference Status* register for the particular channel will be set. The D/S VREF threshold voltage is programmed to a resolution of 10 mv rms. The command is in integer decimal format. For example, if channel 1 input VREF Threshold is to be set for 20.0 Vrms, the command word to the corresponding register would be 2000.

D/S Active Channels

Set the bit, corresponding to each channel to be monitored during BIT testing, in the *Active Channel Register* for the particular D/S channel. "1" = Active; "0" = not used. **IMPORTANT: Omitting this step will produce false alarms because unused channels will set faults.**

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Active Channels	X	X	X	X	X	X	X	X	X	X	X	X	X	CH3	CH2	CH1

D/S Status, Reference Loss

Check the corresponding bit of the *D/S Reference Status Register* for status of the reference input for each active channel. Status is determined by comparing the measured REF input voltage and comparing against the value set in the *VREF Threshold* register. A "1" means Reference is LOST or Not-Applied, "0" means there is a valid Reference applied on active channels. Channels that are inactive are also set to "0". (Reference loss is detected after 2 seconds). Reference monitoring is always enabled. Any D/S reference status failure, transient or intermittent will latch the *D/S Reference Status Register*. Reading will unlatch register.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D/S Status, Reference	X	X	X	X	X	X	X	X	X	X	X	X	X	CH3	CH2	CH1

D/S Status, Phase Lock Loss

Check the corresponding bit of the *D/S Phase Lock Register* for status of the phase lock between the reference input and signal output for each active channel. A "1" means Phase Lock between REF and Signal has been lost, "0" means Phase Lock is sensed on active channels. Channels that are inactive are also set to "0". (Phase Lock loss is detected after 2 seconds). Phase Lock monitoring is always enabled. Any D/S Phase Lock Loss status failure, transient or intermittent will latch the *D/S Phase Lock Loss Status Register*. Reading will unlatch register.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D/S Status, Phase Lock Loss	X	X	X	X	X	X	X	X	X	X	X	X	X	CH3	CH2	CH1

D/S Status, Rotation

Check the corresponding bit of the *D/S Rotation Status Register* for status of rotation (Done or Not Done) for each active channel. A "0" means channel "IN Rotation", "1" means channel "Rotation Stopped" on active channels. Rotation monitoring is always enabled.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D/S Status, Rotation	X	X	X	X	X	X	X	X	X	X	X	X	X	CH3	CH2	CH1

D/S Status, BIT Test Fail

Check the corresponding bit of the *D/S BIT Test Status Register* for status of BIT (Test-Accuracy) Testing for each active channel. A "0" means Accuracy OK; "1" means Accuracy BIT Failed. Accuracy defaulted to +/- 0.2 degrees output as compared to commanded angle. Channels that are inactive are also set to "0". The status bits will be set to indicate an accuracy (0.2º) problem and the results can be read from *D/S Status Registers* within 2 seconds. This test continuously sequences between the channels on the card with each output being measured for approx. 180mSec. If the measured angle has an error greater the 0.05º, a flag will be set in the appropriate register. If the input angle is stepped more then 0.05º during a test cycle, the test cycle will not generally indicate an error. Any D/S test status failure, transient or intermittent will latch the *D/S Test Status Register*. Reading will unlatch register.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D/S Status, BIT Test	X	X	X	X	X	X	X	X	X	X	X	X	X	CH3	CH2	CH1

D/S Status, Signal Loss

Check the corresponding bit of the *D/S Signal Status Register* for status of signal (V_{L-L}). Output signal voltage from each D/S channel is compared against the value set in the *D/S VLL Threshold* register. A "0" means V_{L-L} signal voltage level is OK; "1" means measured signal V_{L-L} voltage "Failed" (below value set in *VLL Threshold* register).

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D/S Status, Signal	X	X	X	X	X	X	X	X	X	X	X	X	X	CH3	CH2	CH1

Oscillator Voltage

The optional On-Board Reference Supply voltage is programmed via the *OSC Voltage* Register. The output reference voltage is programmed to a resolution of 0.1 V(rms). The commanded output word is in integer decimal format. For example, if the optional On-Board Reference Supply is to be programmed to 11.8 V(rms), the commanded word to the register would be 1180 (0x49C).

Oscillator Frequency

The optional On-Board Reference Supply frequency is programmed via the *OSC Frequency* Register. The output reference frequency is programmed to a resolution of 0.1 Hz. The commanded output word is in integer decimal format. For example, if the optional On-Board Reference Supply is to be programmed to 400 Hz, the commanded word to the register would be 4000 (0xFA0).

D/S Test Enable

Set bit to enable associated Built-In Self Test D2 or D3.

The (D2) Test Writing "1" to the D2 bit of the *D/S Test Enable Register* initiates status reporting of the automatic background BIT testing that checks the output accuracy of each channel, by comparing the measured output angle to the commanded angle. The status bits will be set to indicate an accuracy (0.2º) problem and the results can be read from *D/S Status Registers* within 2 seconds. Writing a "0" deactivates the status reporting. The testing is totally transparent to the user, requires no external programming, and has no effect on the standard operation of this card. Note: Outputs must be ON and Reference supplied for test to function. Card will write 55h (every 0.1 seconds) to the *D/S Test (D2) Verify Register* when D2 is enabled. User can periodically clear to 00h and then read the *D/S Test (D2) Verify Register* again, after 0.1 seconds, to verify that BIT Testing is activated. This test continuously sequences between the channels on the card with each output being measured for approx. 180mSec. If the measured angle has an error greater the 0.2º, a flag will be set in the appropriate register. If the input angle is stepped more then 0.05º during a test cycle, the test cycle will not generally indicate an error.

In addition, each D/S Reference input and signal output is continually monitored. Any failure triggers an Interrupt (if enabled) and the results are available in the *D/S Signal* and *D/S Reference Status Registers*.

The (D3) Test Writing "1" to the D3 bit of the *D/S Test Enable Register* initiates a BIT Test that generates and tests 72 different angles to an accuracy of 0.2°. External reference is required and outputs must be ON. The D/S Status bits will be set to indicate an accuracy problem. Results are available in the *D/S Test Status Registers* and if enabled, an interrupt will be generated (See *Interrupt Register*). Test cycle takes about 40 seconds and the D3 bit changes from "1" to "0" when test is complete. The testing requires no external programming, and can be terminated at any time by writing a "0" to the D3 bit of the *D/S Test Enable Register*.

CAUTION: Outputs must be ON and Reference must be supplied during this test (D3) and therefore are active. Check connected loads for possible interaction.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Test Enable	X	X	X	X	X	X	X	X	X	X	X	X	D3	D2	X	X

DIGITAL I/O FUNCTIONS

I/O Select

Individually controls the digital I/O (Input/Output) channel direction selection. A "0" in the channel Bank Select Register sets the corresponding channel to be Inputs. A "1" sets the corresponding channel in the bank to be Outputs.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
I/O Select	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT

Input Register

Indicates the logic state of Digital I/O bits. Lower byte represents bank 0-7.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Input State	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT

Output Register

Controls the logic state of Digital I/O's, when bank is set to be Outputs. Lower byte controls bank 0-7.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Output State	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT

MODULE IDENTIFICATION

Module Design Version

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design version in ASCII. For example, ASCII "1" in upper byte and ASCII space in lower byte for Module Design Version "1 " is together 3120h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE SPECIAL SPEC	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "1"								ASCII " "								

Module Design Revision

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design revision code in ASCII. For example, ASCII "B" in upper byte and ASCII space in lower byte for Module Design Revision "B " is together 4220h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN REVISION	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "B"								ASCII " "								

Module DSP

Type: binary word
Range: 1 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module DSP revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DSP	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module FPGA

Type: binary word
Range: 1 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module FPGA revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE FPGA	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module ID (Part Number)

Type: binary word
Range: N/A
Read/Write: R
Initialized Value: N/A

Read as 16 BIT Binary Word

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Mod ID (Part Number)	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Serial Number

Read as 16 BIT Binary Word

Date Code

Read as a decimal number. The four digits represent YYWW (Year, Year, Week, Week)

Watchdog Timer

This feature monitors the watchdog timer register. When it detects that a code has been received, that code will be inverted within 100 µSec. The inverted code stays in the register until replaced by a new code. After 100 µSec. elapse, look for the inverted code to confirm that the processor is operating.

Soft Reset

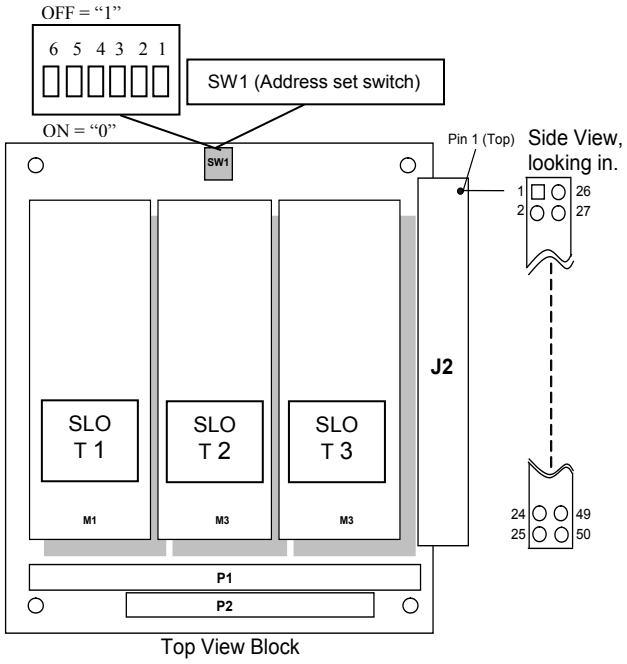
Soft Reset is Level sensitive. Writing a "1" initiates and holds software in reset state; then writing "0" initiates reboot (depending upon configuration, takes up to 3 seconds). This function is equivalent to a power-on reset where all parameters are reset to their default condition.

Test (D2) Verify

Card will (every 100 ms) write 55h at Test (D2) Verification register when (D2) is enabled. User can periodically clear to 00h and then read again, after (100 ms), to verify that background bit testing is activated.

MECHANICAL

PC104, General Layout



Top View Block

I/O CONNECTOR PINOUT

J2 I/O Connector: Harwin M80-5415022; Mate: Harwin M80-486 product family

Pin		Pin	
1	Ch.1-S1	26	Ch.1- Sense S1
2	Ch.1-S3	27	Ch.1- Sense S3
3	Ch.1-S2	28	Ch.1- Sense S2
4	Ch.1-S4	29	Ch.1- Sense S4
5	Ch.1-RHi	30	Ch.1-RLo
6	N/C	31	N/C
7	Ch.2-S1	32	Ch.2- Sense S1
8	Ch.2-S3	33	Ch.2- Sense S3
9	Ch.2-S2	34	Ch.2- Sense S2
10	Ch.2-S4	35	Ch.2- Sense S4
11	Ch.2-RHi	36	Ch.2-RLo
12	N/C	37	N/C
13	Ch.3-S1 (Ref Out Lo) *1	38	Ch.3- Sense S1
14	Ch.3-S3 (Ref Out Hi) *1	39	Ch.3- Sense S3
15	Ch.3-S2	40	Ch.3- Sense S2
16	Ch.3-S4	41	Ch.3- Sense S4
17	Ch.3-RHi	42	Ch.3-RLo
18	AGND	43	AGND
19	+12V Ext	44	+12V Ext
20	-12V Ext	45	-12V Ext
21	AGND	46	AGND
22	DIO0	47	DIO1
23	DIO2	48	DIO3
24	DIO4	49	DIO5
25	DIO6	50	DIO7

*1 - When specified; Optional On-Board Reference supply output in lieu of Channel 3 D/S-R (see part number)

NAI Synchro / Resolver naming convention:

Signal	Resolver	Synchro
S1	SIN(-)	X
S2	COS(+)	Z
S3	SIN(+)	Y
S4	COS(-)	(No connect)

PART NUMBER DESIGNATION

73DS2 - XX XX XX X X - XX

Slot 1
(Enter code - See module configurator)
(Enter **Z0** if not populated)

Slot 2
(Enter code - See module configurator)
(Enter **Z0** if not populated)

Slot 3
(Enter code - See module configurator)
*1 May be populated with programmable Reference Source
(Enter **Z0** if not populated)

ENVIRONMENTAL
C = No Conformal Coating
K = Removable Conformal Coating

CODE
(Reserved for special configurations – leave open for standard

OPTIONS
0 = None (configured for bus powered +/- 12 VDC)*2
1 = Configured for external +/- 12 VDC*2
9 = Custom Design (See Separate Spec)

MODULE CONFIGURATOR

(single channel)

Code	Format	V_{L-L} (V_{RMS})	V_{REF} (V_{RMS})	Freq (Hz)	Power (VA)	Remarks
70	SYN	2 - 11.8	2 – 28	400 – 1K	1.2	
71	RSL	2 - 11.8	2 – 28	400 – 1K	1.2	
72	RSL	2 - 28	2 – 28	400 – 1K	1.2	
73	SYN	90	28 – 115	400 – 1K	1.2	
74	RSL	90	28 – 115	400 – 1K	1.2	
75	SYN	11.8	2 – 28	47 - 440	1.2	
76	RSL	2 - 11.8	2 – 28	47 - 440	1.2	
77	RSL	2 - 28	2 – 28	47 - 440	1.2	
78	SYN	90	28 – 115	47 - 440	1.2	
79	RSL	90	28 – 115	47 - 440	1.2	
7A	RSL	2 - 11.8	2 – 28	1K – 3K	1.2	
7B	RSL	2 - 11.8	2 – 28	3K – 5K	1.2	
7C	RSL	2 - 11.8	2 – 28	5K – 7K	1.2	
7D	RSL	2 - 11.8	2 – 28	7K – 10K	1.2	
7E	RSL	2 – 28	2 – 28	1K – 3K	1.2	
7F	RSL	2 – 28	2 – 28	3K – 5K	1.2	
7G	RSL	2 – 28	2 – 28	5K – 7K	1.2	
7H	RSL	2 – 28	2 – 28	7K – 10K	1.2	
W4	PROG REF	2 – 28		47 – 10K	3.0	May only be specified in Slot 3*1
W5	PROG REF	28 - 115		47 – 10K	3.0	May only be specified in Slot 3*1

Part Numbering Notes:

*1 When specified; Optional On-Board Reference supply output in lieu of Channel 3 D/S-R.

*2 The card, by default (code "0" for options designator), is set-up for receiving +/-12 VDC from the PC/104 bus power. In some applications where bus power is limited or if a separate power supply is required, the card at time of order, can be configured for receiving +/-12 VDC from an external (bus power isolated) source (code "1" for options designator).

REVISION PAGE

Revision	Description of Change	Engineer	Date
5.0	Based on 73_DS2_A001_Rev_4.0 / New feature programmability requires clarifications / BIO requires definitions	AS	8/23/07
5.1	Preliminary Release – Continuing clarifications	AS	8/27/07
5.2	Clarifications – Register specific Hi/Lo for Wrap, Angle, Ref V, Sig VLL, OSC, ROT Rate, swapped/corrected; Added register functions phase accum, compile time, signal status; Various typos corrected.	AS	9/24/07
5.3	Updated power requirements / redefined part number configurator for D/S channel options	AS	9/25/07
5.4	Updated with new part numbering configurator; Reg map corrections	AS	11/27/07
A	Initial release to Agile	AS	12/03/07
A1	Pending to Agile / minor corrections	AS	12/11/07
A2	Release to Agile / Clarifications to module power	AS	3/25/08
A3	Re-release to Agile / Clarified module slots and address switch layout	AS	3/28/08
A4	Revised Temperature Specs	AS	1/06/10